WHAT IS CLAIMED IS:

1. A circuit modification method of modifying a circuit by inserting one or more buffers into a predetermined wire located within the circuit, the method comprising the steps of:

determining whether a glitch error is caused in said predetermined wire by one or more aggressors each comprised of one or more other wires;

when determining that a glitch error is caused in said predetermined wire by one or more aggressors, determining one or more positions where one or more buffers are to be inserted into said predetermined wire based on a coupling capacity between each of said one or more aggressors and said predetermined wire.

2. The circuit modification method according to Claim 1, wherein said insertion position determining step includes the steps of, when determining that a glitch error is caused in said predetermined wire by only one aggressor, calculating a target coupling capacity using the coupling capacity between said aggressor and said predetermined wire, and, when dividing said predetermined wire into a plurality of wire segments, determining one or more internal points of division of said predetermined wire so that a coupling capacity between each of said plurality of wire segments and said aggressor does not exceed said target coupling capacity, and setting said one or more internal points of division to said one or more positions where said one or more buffers are to be inserted into said

predetermined wire.

3. The circuit modification method according to Claim 2, wherein said target coupling capacity calculating step is the step of calculating said target coupling capacity by using an amount of glitch to be caused in said predetermined wire by said aggressor.

4. The circuit modification method according to Claim 3, wherein said target coupling capacity calculating step includes the steps of determining the number of said plurality of wire segments based on said amount of glitch, and calculating said target coupling capacity based on said coupling capacity between said aggressor and said predetermined wire and the number of said plurality determined in the above step.

5. The circuit modification method according to Claim 4, wherein said wire segment number determining step is the step of, when the coupling capacity between said aggressor and said predetermined wire is Cc, said amount of glitch is V, and a predetermined value is Vmax, determining the smallest integer number n which satisfies a following relationship: V/n Vmax as the number of said plurality of wire segments, and wherein said target coupling capacity calculating step is the step of calculating said target coupling capacity as follows: Cc/n, and said internal division point determining step is the step of determining said one or more internal points of division so that the coupling capacity between each of said plurality of wire

segment and said aggressor is equal to said target coupling capacity Cc/n.

6. The circuit modification method according to Claim 3, wherein said target coupling capacity calculating step is the step of, when the coupling capacity between said aggressor and said predetermined wire is Cc, said amount of glitch is V, and a predetermined value is Vmax, calculating said target coupling capacity as follows: Cc*Vmax/V.

7. The circuit modification method according to Claim 1, wherein said one or more buffers to be inserted into said predetermined wire have a driving ability equal to or greater than that of a driving circuit for driving said predetermined wire.

8. The circuit modification method according to Claim 7, further comprising the step of selecting a type of buffer having a driving ability equal to or greater than that of said driving circuit for driving said predetermined wire and having a minimum area as each of said one or more buffers to be inserted into said predetermined wire from among a plurality of buffer cells stored in a cell library.

9. The circuit modification method according to Claim 1, further comprising the steps of, when determining that a glitch error is caused in said predetermined wire by one or more aggressors, replacing a driving circuit for driving said predetermined wire with another one having a higher driving ability than the driving circuit, and, before

performing said insertion position determining step, determining whether a glitch error is caused in said predetermined wire driven by the other driving circuit by said one or more aggressors.

10. The circuit modification method according to Claim 1, wherein said insertion position determining step includes the steps of, when determining that a glitch error is caused in said predetermined wire by a plurality of aggressors, calculating a plurality of target coupling capacities respectively associated with said plurality of aggressors by using the coupling capacity between each of said plurality of aggressors and said predetermined wire, and, when dividing said predetermined wire into a plurality of wire segments, determining one or more internal points of division of said predetermined wire so that a coupling capacity between each of said plurality of wire segments and each of said plurality of aggressors does not exceed a corresponding one of said plurality of target coupling capacities, and setting said one or more internal points of division to said one or more positions where said one or more buffers are to be inserted into said predetermined wire.

11. The circuit modification method according to Claim 10, wherein said target coupling capacity calculating step includes the steps of, when the coupling capacity between each of said plurality of aggressors (referred to as *ith* (i=1 to k, k is the number of aggressors) aggressor hereafter) and said predetermined wire is Cc_i (i=1 to k),

an amount of glitch to be caused in said predetermined wire by the *ith* aggressor is V_i (i=1 to k), and a predetermined value is Vmax, determining the smallest integer number n_i (i=1 to k) which satisfies a following relationship: V_i/n_i Vmax (i=1 to k) as the number of said plurality of wire segments for each of said plurality of aggressors, and calculating each of said plurality of target coupling capacities as follows: Cc_i/n_i (i=1 to k).

12. The circuit modification method according to Claim 10, wherein said insertion position determining step includes the steps of when dividing said predetermined wire into a plurality of wire segments for each of said plurality of aggressors, determining said one or more internal points of division of said predetermined wire so that the coupling capacity between each of said plurality of wire segment and each of said plurality of aggressor is equal to said corresponding target coupling capacity, and selecting said one or more positions where one or more buffers to be inserted into said predetermined wire from among all internal points of division determined in the above step for said plurality of aggressors.

13. The circuit modification method according to Claim 11, wherein said insertion position determining step includes the steps of when dividing said predetermined wire into a plurality of wire segments for each of said plurality of aggressors, i.e., said *ith* aggressor, determining said one or more internal points of division of said predetermined wire so that the coupling capacity

between each of said plurality of wire segment and said *ith* aggressor is equal to said corresponding target coupling capacity Cc_i/n_i (i=1 to k), and selecting said one or more positions where one or more buffers to be inserted into said predetermined wire from among all internal points of division determined in the above step for said plurality of aggressors.

14. The circuit modification method according to Claim 10, wherein said target coupling capacity calculating step includes the steps of, when the coupling capacity between each of said plurality of aggressors (referred to as *ith* (i=1 to k, k is the number of aggressors) aggressor hereafter) and said predetermined wire is Cc_i (i=1 to k), an amount of glitch to be caused in said predetermined wire by said *ith* aggressor is V_i (i=1 to k), and a predetermined value is Vmax, calculating each of said plurality of target coupling capacities as follows: Cc_i*Vmax/V_i (i=1 to k).

15. A circuit modification method of modifying a circuit by inserting one or more buffers into a predetermined wire located within the circuit, the method comprising the steps of:

determining whether a glitch error is caused in said predetermined wire by an aggressor comprised of one or more other wires;

when determining that a glitch error is caused in said predetermined wire by an aggressor, determining a number of buffers to be inserted into said predetermined wire based on an amount of glitch to be caused in said

predetermined wire by said aggressor.

16. The circuit modification method according to Claim 15, wherein said buffer number determining step is the step of, when said amount of glitch is V and a predetermined value is Vmax, calculating the smallest integer number n which satisfies a following relationship: V/n Vmax.

17. The circuit modification method according to Claim 15, wherein said one or more buffers to be inserted into said predetermined wire have a driving ability equal to or greater than that of a driving circuit for driving said predetermined wire.

18. The circuit modification method according to Claim 17, further comprising the step of selecting a type of buffer having a driving ability equal to or greater than that of said driving circuit for driving said predetermined wire and having a minimum area as each of said one or more buffers to be inserted into said predetermined wire from among a plurality of buffer cells stored in a cell library.

19. The circuit modification method according to Claim 15, further comprising the steps of, when determining that a glitch error is caused in said predetermined wire by one aggressor, replacing a driving circuit for driving said predetermined wire with another one having a higher driving ability than the driving circuit, and, before performing said buffer number determining step, determining whether a

glitch error is caused in said predetermined wire driven by the other driving circuit by said one aggressor.

20. A circuit modification method comprising the steps of:

determining whether a glitch error is caused in said predetermined wire by an aggressor comprised of one or more other wires;

when determining that a glitch error is caused in said predetermined wire by an aggressor, replacing a driving circuit for driving said predetermined wire with another one having a higher driving ability than the driving circuit.